

Rakesh Chadha · J. Bhasker

An ASIC Low Power Primer

Analysis, Techniques and Specification

 Springer

An Asic Low Power Primer Analysis Techniques And Specification

Navya Sree Paleru



An Asic Low Power Primer Analysis Techniques And Specification:

An ASIC Low Power Primer Rakesh Chadha,J. Bhasker,2012-12-05 This book provides an invaluable primer on the techniques utilized in the design of low power digital semiconductor devices Readers will benefit from the hands on approach which starts from the ground up explaining with basic examples what power is how it is measured and how it impacts on the design process of application specific integrated circuits ASICs The authors use both the Unified Power Format UPF and Common Power Format CPF to describe in detail the power intent for an ASIC and then guide readers through a variety of architectural and implementation techniques that will help meet the power intent From analyzing system power consumption to techniques that can be employed in a low power design to a detailed description of two alternate standards for capturing the power directives at various phases of the design this book is filled with information that will give ASIC designers a competitive edge in low power design

Introduction to VLSI Design Flow Sneh Saurabh,2023-06-15 Chip designing is a complex task that requires an in depth understanding of VLSI design flow skills to employ sophisticated design tools and keeping pace with the bleeding edge semiconductor technologies This lucid textbook is focused on fulfilling these requirements for students as well as a refresher for professionals in the industry It helps the user develop a holistic view of the design flow through a well sequenced set of chapters on logic synthesis verification physical design and testing Illustrations and pictorial representations have been used liberally to simplify the explanation Additionally each chapter has a set of activities that can be performed using freely available tools and provide hands on experience with the design tools Review questions and problems are given at the end of each chapter to revise the concepts Recent trends and references are listed at the end of each chapter for further reading

Green Technology for Smart City and Society Renu Sharma,Manohar Mishra,Janmenjoy Nayak,Bighnaraj Naik,Danilo Pelusi,2020-11-30 This book includes selected papers from the International Conference on Green Technology for Smart City and Society GTSCS 2020 organized by the Institute of Technical Education and Research Siksha O Anusandhan University Bhubaneswar India during 13 14 August 2020 The book covers topics such as machine learning artificial intelligence deep learning optimization algorithm IoT signal processing etc The book is helpful for researchers working in the discipline of Electrical Electronics and Computer Science The researchers working in the allied domain of communication and control will also find the book useful as it deals with the latest methodologies and applications

An ASIC Low Power Primer Springer,2012-12-06 *Closing the Power Gap between ASIC & Custom* David Chinnery,Kurt Keutzer,2008-01-23 Explains how to use low power design in an automated design flow and examine the design time and performance trade offs Includes the latest tools and techniques for low power design applied in an ASIC design flow Focuses on low power in an automated design methodology a much neglected area

Implementation of Complete Application-specific Integrated Circuits Design Using Low Power Methodology Mehran Amrbar,2012 In today s technological advancements in VLSI industry the limits of ASICs FPGA chips in terms of area power and speed are

constantly shrinking The end user requirements are also influencing these limits and pushing them to a new level on top of all these technological advancements The effects of nanometer technologies on congestion signal integrity crosstalk etc are becoming more significant as the technology sizes of semiconductor devices continue to decrease All of these factors are affecting and forcing various technological methodologies throughout the design flow to constantly fight and keep updating the EDA tools to cop up with these issues Thus there is always a need of constant learning and exposure to new advanced EDA tools like Synopsys Design Compiler IC Compiler PrimeTime TetraMax etc The aim of this project is to successfully complete the ASIC design flow with low power techniques using the advance industry level tools This project provides a solid base and practical hands on experience of these advanced tools It also provides an overview of types of ASICs detailed ASIC standard design flow and Synopsys IC compiler flow Along with this the analysis of various design factors affecting the performance of the final chip such as power area and timing is also performed In this project a RISC CHIP from Synopsys will be used to perform ASIC design flow and low power methodology

An ASIC Power Analysis System for Digital CMOS Design Du Van Nguyen,1997 *Physical Design Essentials* Khosrow Golshan,2007-04-08 Arranged in a format that follows the industry common ASIC physical design flow Physical Design Essentials begins with general concepts of an ASIC library then examines floorplanning placement routing verification and finally testing Among the topics covered are Basic standard cell design transistor sizing and layout styles Linear non linear and polynomial characterization Physical design constraints and floorplanning styles Algorithms used for placement Clock Tree Synthesis Parasitic extraction Electronic Testing and many more

Low Power ASIC Design Using 90NM Technology Sunil Kumar Aluri,2010 *Closing the Gap Between ASIC & Custom* David Chinnery,Kurt William Keutzer,2002 This book carefully details design tools and techniques for high performance ASIC design Using these techniques the performance of ASIC designs can be improved by two to three times Important topics include Improving performance through microarchitecture Timing driven floorplanning Controlling and exploiting clock skew High performance latch based design in an ASIC methodology Automatically identifying and synthesizing complex logic gates Automated cell sizing to increase performance and reduce power Controlling process variation These techniques are illustrated by designs running two to three times the speed of typical ASICs in the same process generation

Low Power ASIC Design Using 90nm Technology Shilpa Jammula,2008 *Specification Analysis for System-level Power-aware ASIC Design* David Ariel Lemma,2021 The field of Electronic Design Automation EDA is a growing field whose growth is fueled among many factors by the ever increasing number of Application Specific Integrated Circuits ASIC that are required by digital systems Amidst the current explosion in the design and production of Internet of Things IoT typically battery powered devices the need for power aware design has reached critical importance The need for a holistic view power aware of the implications and challenges brought forth by the need to curb and properly manage power consumption power has revealed a need for the EDA field to explore system level top down based methodologies As a

response to the needs this document presents two frameworks based on specification analysis at the system level in order to address the holistic view of power aware design One of the frameworks focuses on system level specifications written in natural language ie English whereas the other focuses on system level specifications written in a technical language ie SystemC The frameworks are shown to be able to analyze these types of system level specifications so as to aid designers in power aware ASIC design These frameworks encapsulate the contributions of this thesis which are defined by the proper devising of analytical rules to parse the system level specification so as to extract the basic underlying Power Management Strategy PMS laid out of by the specification under analysis Use cases show the effectiveness of the frameworks in aiding designers targetting typical ASIC elements such as a bus a port processor encoders and a processor centric programmable System on Chip SoC all of them typical components of IoT devices The document ends with a conclusion summarizing the work and pointing to possible future extensions to the frameworks and general research lines that are possible avenues for developments in the field of specification analysis for power aware system level ASIC design

Low Power ASIC Design Ramin Alebouyeh,2009 Low Power ASIC Design Using Voltage Scaling at the Logic Level Torsten Mahnke,2003 **Low Power ASIC Design** Richard Conrad Ross,2008 **Low Power ASIC Design Using Synopsys Tools** Rashma Madhavaram,2010 *Low Power ASIC Design Flow Using Synopsys Tool* Navya Sree Paleru,2010 **Low Power Design with High-Level Power Estimation and Power-Aware Synthesis** Sumit Ahuja,Avinash Lakshminarayana,Sandeep Kumar Shukla,2011-10-21 This book presents novel research techniques algorithms methodologies and experimental results for high level power estimation and power aware high level synthesis Readers will learn to apply such techniques to enable design flows resulting in shorter time to market and successful low power ASIC FPGA design

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