

EXPERIMENT No.1
REALIZATION OF GATES USING UNIVERSAL GATES

AIM: To verify all gates using NAND and NOR gates.

APPARATUS: Breadboard, IC 7400 (NAND), IC 7402(NOR), LEDs, +5V power supply Connecting wires.

THEORY: NAND Gate: The NAND gate represents the complement of the AND operation. Its name is an abbreviation of NOT AND. The graphic symbol for the NAND gate consists of an AND symbol with a bubble on the output, denoting that a complement operation is performed on the output of the AND gate as shown in Fig 1.1



X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

Fig 1.1 NAND gate

NOR Gate: The NOR gate represents the complement of the OR operation. Its name is an abbreviation of NOT OR. The graphic symbol for the NOR gate consists of an OR symbol with a bubble on the output, denoting that a complement operation is performed on the output of the OR gate. The truth table and the graphic symbol of NOR gate is shown in the fig 1.2.



X	Y	NOR
0	0	1
0	1	0
1	0	0
1	1	0

Fig 1.2 NOR gate

NAND and NOR Gates are called as universal gates as all other gates can be implemented using these two gates.

Btech Digital Design Laboratory Manual

Richard F. Tinder

Btech Digital Design Laboratory Manual:

Digital Design Thomas Collins,Christopher Twigg,2009 ELECTRONICS LAB MANUAL (VOLUME 2) NAVAS, K. A.,2018-10-01 This book is evolved from the experience of the author who taught all lab courses in his three decades of teaching in various universities in India The objective of this lab manual is to provide information to undergraduate students to practice experiments in electronics laboratories This book covers 118 experiments for linear analog integrated circuits lab communication engineering lab power electronics lab microwave lab and optical communication lab The experiments described in this book enable the students to learn Various analog integrated circuits and their functions Analog and digital communication techniques Power electronics circuits and their functions Microwave equipment and components Optical communication devices This book is intended for the B Tech students of Electronics and Communication Engineering Electrical and Electronics Engineering Biomedical Electronics Instrumentation and Control Computer Science and Applied Electronics It is designed not only for engineering students but can also be used by BSc MSc Physics and Diploma students

KEY FEATURES Contains aim components and equipment required theory circuit diagram pin outs of active devices design tables graphs alternate circuits and troubleshooting techniques for each experiment Includes viva voce and examination questions with their answers Provides exposure on various devices

TARGET AUDIENCE B Tech Electronics and Communication Engineering Electrical and Electronics Engineering Biomedical Electronics Instrumentation and Control Computer Science and Applied Electronics BSc MSc Physics Diploma Engineering

Readings in Hardware/Software Co-Design Giovanni De Micheli,Rolf Ernst,Wayne Wolf,2001-06-19 Embedded system designers are constantly looking for new tools and techniques to help satisfy the exploding demand for consumer information appliances and specialized industrial products One critical barrier to the timely release of embedded system products is integrating the design of the hardware and software systems Hardware software co design is a set of methodologies and techniques specifically created to support the concurrent design of both systems effectively reducing multiple iterations and major redesigns In addition to its critical role in the development of embedded systems many experts believe that co design will be a key design methodology for Systems on a Chip Readings in Hardware Software Co Design presents the papers that have shaped the hardware software co design field since its inception in the early 90s Field experts Giovanni De Micheli Rolf Ernst and Wayne Wolf introduce sections of the book and provide context for the paper that follow This collection provides professionals researchers and graduate students with a single reference source for this critical aspect of computing design Over 50 peer reviewed papers written from leading researchers and designers in the field Selected edited and introduced by three of the fields most eminent researchers and educators Accompanied by an annually updated companion Web site with links and references to recently published papers providing a forum for the editors to comment on how recent work continues or breaks with previous work in the field

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Technically up to date this book covers all the latest topics Field programmable gate arrays PALs and ROMs The latest memory chips for SRAM and DRAM are shown Software for creating the excitation equations of FSM are covered as well as LogicWorks and Beige Bag PC and more **IEICE Transactions on Electronics** ,1994 Digital Electronics Cherry Bhargava,2020-06

Transactions of the Society for Modeling and Simulation International ,2000 *Proceedings of the 8th International Conference on VLSI Design, January 4-7, 1995, New Delhi, India* ,1995 Presents papers from the January 1995 conference Topics include routing hardware software design CAD sequential automatic test pattern generation logic synthesis VLSI arithmetic and chip design Includes tools and technology poster sessions and a panel discussion on India's role in the VLSI w

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International Symposium on VLSI Design ,1995 **Marquis International Who's who in Optical Science and Engineering** ,1985 Digital Circuit Design Laboratory Manual, 4th edition (Global) Akhan Almagambetov,J. Matt

Pavlina,Yelena Mukhortova, **Nuclear Science Abstracts** ,1973 **Digital Circuit Design Laboratory Manual** John Matthew Pavlina,Yelena Leonidovna Mukhortova,Akhan Almagambetov,2020-05-23 Laboratory manual for Digital Circuit Design using Intel Quartus software Suitable for online and in person instruction Required for Embry Riddle Aeronautical University classes Includes the following laboratories 1 Introduction to Digital Circuits Lab 2 FPGA Design Workflow 3 Combinational Logic Circuits 4 Seven segment Display Logic 5 Combinational Logic using VHDL 6 Multiplexed Displays 7 Servo Motor Control 8 Accelerometer Interfacing 9 SPDT Switch Debouncing Multiplexers 10 Brushless DC Motor Control Covers the following topics in the appendices Basic Electrical Components HDL Design Using Intel Quartus Using Symbolic Blocks in Intel Quartus Multiplexing Pulse Width Modulation PWM Functional Simulation using ModelSim Has the following references in the appendices Development Board Pin Listings VHDL Source Code Listing Device Data

Who's Who in Science and Engineering 2008-2009 Who's Who Marquis,Marquis Who's Who,2007-12 Engineering Digital Design

Richard F. Tinder,2000-01-18 Engineering Digital Design Second Edition provides the most extensive coverage of any available textbook in digital logic and design The new REVISED Second Edition published in September of 2002 provides 5

productivity tools free on the accompanying CD ROM This software is also included on the Instructor s Manual CD ROM and complete instructions accompany each software program In the REVISED Second Edition modern notation combines with state of the art treatment of the most important subjects in digital design to provide the student with the background needed to enter industry or graduate study at a competitive level Combinatorial logic design and synchronous and asynchronous sequential machine design methods are given equal weight and new ideas and design approaches are explored The productivity tools provided on the accompanying CD are outlined below 1 EXL Sim2002 logic simulator EXL Sim2002 is a full featured interactive schematic capture and simulation program that is ideally suited for use with the text at either the entry or advanced level of logic design Its many features include drag and drop capability rubber banding mixed logic and positive logic simulations macro generation individual and global or randomized delay assignments connection features that eliminate the need for wire connections schematic page sizing and zooming waveform zooming and scrolling a variety of printout capabilities and a host of other useful features 2 BOOZER logic minimizer BOOZER is a software minimization tool that is recommended for use with the text It accepts entered variable EV or canonical 1 s and 0 s data from K maps or truth tables with or without don t cares and returns an optimal or near optimal single or multi output solution It can handle up to 12 functions Boolean functions and as many inputs when used on modern computers 3 ESPRESSO II logic minimizer ESPRESSO II is another software minimization tool widely used in schools and industry It supports advanced heuristic algorithms for minimization of two level multi output Boolean functions but does not accept entered variables It is also readily available from the University of California Berkeley 1986 VLSI Tools Distribution 4 ADAM design software ADAM for Automated Design of Asynchronous Machines is a very powerful productivity tool that permits the automated design of very complex asynchronous state machines all free of timing defects The input files are state tables for the desired state machines The output files are given in the Berkeley format appropriate for directly programming PLAs ADAM also allows the designer to design synchronous state machines timing defect free The options include the lumped path delay LPD model or NESTED CELL model for asynchronous FSM designs and the use of D FLIP FLOPs for synchronous FSM designs The background for the use of ADAM is covered in Chapters 11 14 and 16 of the REVISED 2nd Edition 5 A OPS design software A OPS for Asynchronous One hot Programmable Sequencers is another very powerful productivity tool that permits the design of asynchronous and synchronous state machines by using a programmable sequencer kernel This software generates a PLA or PAL output file in Berkeley format or the VHDL code for the automated timing defect free designs of the following a Any 1 Hot programmable sequencer up to 10 states b The 1 Hot design of multiple asynchronous or synchronous state machines driven by either PLDs or RAM The input file is that of a state table for the desired state machine This software can be used to design systems with the capability of instantly switching between several radically different controllers on a time shared basis The background for the use of A OPS is covered in Chapters 13 14 and 16 of the REVISED 2nd Edition

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