Accelerating Test, Validation and Debug of High Speed Serial Interfaces

Accelerating Test Validation And Debug Of High Speed Serial Interfaces

Yongquan Fan,Zeljko Zilic

Accelerating Test Validation And Debug Of High Speed Serial Interfaces:

Accelerating Test, Validation and Debug of High Speed Serial Interfaces Yongquan Fan,Zeljko Zilic,2010-10-20 High Speed Serial Interface HSSI devices have become widespread in communications from the embedded to high performance computing systems and from on chip to a wide haul Testing of HSSIs has been a challenging topic because of signal integrity issues long test time and the need of expensive instruments Accelerating Test Validation and Debug of High Speed Serial Interfaces provides innovative test and debug approaches and detailed instructions on how to arrive to practical test of modern high speed interfaces Accelerating Test Validation and Debug of High Speed Serial Interfaces first proposes a new algorithm that enables us to perform receiver test more than 1000 times faster Then an under sampling based transmitter test scheme is presented The scheme can accurately extract the transmitter jitter and finish the whole transmitter test within 100ms while the test usually takes seconds The book also presents and external loopback based testing scheme where and FPGA based BER tester and a novel jitter injection technique are proposed These schemes can be applied to validate test and debug HSSIs with data rate up to 12 5Gbps at a lower test cost than pure ATE solutions In addition the book introduces an efficieng scheme to implement high performance Gaussian noise generators suitable for evaluating BER performance under noise conditions **Accelerating Test, Validation and Debug of High Speed Serial Interfaces** Fan Yongquan,Zeljko Zilic,2011-07-16 High Speed Serial Interface HSSI devices have become widespread in communications from the embedded to high performance computing systems and from on chip to a wide haul Testing of HSSIs has been a challenging topic because of signal integrity issues long test time and the need of expensive instruments Accelerating Test Validation and Debug of High Speed Serial Interfaces provides innovative test and debug approaches and detailed instructions on how to arrive to practical test of modern high speed interfaces Accelerating Test Validation and Debug of High Speed Serial Interfaces first proposes a new algorithm that enables us to perform receiver test more than 1000 times faster Then an under sampling based transmitter test scheme is presented The scheme can accurately extract the transmitter jitter and finish the whole transmitter test within 100ms while the test usually takes seconds The book also presents and external loopback based testing scheme where and FPGA based BER tester and a novel jitter injection technique are proposed These schemes can be applied to validate test and debug HSSIs with data rate up to 12 5Gbps at a lower test cost than pure ATE solutions In addition the book introduces an efficieng scheme to implement high performance Gaussian noise generators suitable for evaluating BER performance under noise conditions **An Engineer's Guide to Automated Testing of High-Speed Interfaces, Second Edition** Jose Moreira,Hubert Werkmann,2016-04-30 This second edition of An Engineer s Guide to Automated Testing of High Speed Interfaces provides updates to reflect current state of the art high speed digital testing with automated test equipment technology ATE Featuring clear examples this one stop reference covers all critical aspects of automated testing including an introduction to high speed digital basics a discussion of

industry standards ATE and bench instrumentation for digital applications and test and measurement techniques for characterization and production environment Engineers learn how to apply automated test equipment for testing high speed digital I O interfaces and gain a better understanding of PCI Express 4 100Gb Ethernet and MIPI while exploring the correlation between phase noise and jitter This updated resource provides expanded material on 28 32 Gbps NRZ testing and wireless testing that are becoming increasingly more pertinent for future applications This book explores the current trend of merging high speed digital testing within the fields of photonic and wireless testing **Electrical & Electronics Abstracts** ,1997 *Efficient Test Methodologies for High-Speed Serial Links* Dongwoo Hong,Kwang-Ting Cheng,2009-12-24 Efficient Test Methodologies for High Speed Serial Links describes in detail several new and promising techniques for cost effectively testing high speed interfaces with a high test coverage One primary focus of Efficient Test Methodologies for High Speed Serial Links is on efficient testing methods for jitter and bit error rate BER which are widely used for quantifying the quality of a communication system Various analysis as well as experimental results are presented to demonstrate the validity of the presented techniques *Efficient Test Methodologies for High-Speed Serial Links* Hong Dongwoo,Kwang-Ting Cheng,2010-05-05 Efficient Test Methodologies for High Speed Serial Links describes in detail several new and promising techniques for cost effectively testing high speed interfaces with a high test coverage One primary focus of Efficient Test Methodologies for High Speed Serial Links is on efficient testing methods for jitter and bit error rate BER which are widely used for quantifying the quality of a communication system Various analysis as well as experimental results are presented to demonstrate the validity of the presented techniques An Engineer's Guide to Automated Testing of High-speed Interfaces José Moreira,Hubert Werkmann,2010 Providing a complete introduction to the state of the art in high speed digital testing with automated test equipment ATE this practical resource is the first book focus exclusively on this increasingly important topic Featuring clear examples this one stop reference covers all critical aspects of the subject from high speed digital basics ATE instrumentation for digital applications and test and measurements to production testing support instrumentation and text fixture design This in depth volume also discusses at advanced ATE topics such as multiplexing of ATE pin channels and testing of high speed bi directional interfaces with fly by approaches Signal Integrity Validation for High-speed Serial Links Alex Messan,2005 Post-Silicon Validation and Debug Prabhat Mishra,Farimah Farahmandi,2018-09-01 This book provides a comprehensive coverage of System on Chip SoC post silicon validation and debug challenges and state of the art solutions with contributions from SoC designers academic researchers as well as SoC verification experts The readers will get a clear understanding of the existing debug infrastructure and how they can be effectively utilized to verify and debug SoCs **Cost Effective Tests for High Speed I/O Subsystems** Ji Hwan Chun,2011 The growing demand for high performance systems in modern computing technology drives the development of advanced and high speed designs in I O structures Due to their data rate and architecture however testing of the high speed serial interfaces becomes more

expensive when using conventional test methods In order to alleviate the test cost issue a loopback test scheme has been widely adopted To assess the margin of the signal eye in the loopback configuration the eye margin is purposely reduced by additional devices on the loopback path or using design for testability DFT features such as timing and voltage margining Although the loopback test scheme successfully reduces the test cost by decoupling the dependency of external test equipment it has robustness issues such as a fault masking issue and a non ideality problem of margining circuits The focus of this dissertation is to propose new methods to resolve the known issues in the loopback test mode The fault masking issue in a loopback pair of analog to digital and digital to analog converters ADC and DAC which can be found in pulse amplitude modulation PAM signaling schemes is resolved using a proposed algorithm which separates the characteristics of the ADC and the DAC from a combined loopback response The non ideality problem of margining circuit is resolved using a proposed method which utilizes a random jitter injection technique Using the injected random jitter the jitter distribution is sampled by undersampling and margining which provides the nonlinearity information using the proposed algorithm Since the proposed method requires a random jitter source on the load board an alternative solution is proposed which uses an intrinsic jitter profile and a sliding window search algorithm to characterize the nonlinearities The sliding search algorithm was implemented in a low cost high volume manufacturing HVM tester to assess feasibility and validity of the proposed technique The proposed methods are compatible with the existing loopback test scheme and require a minimal area and design overhead hence they provide cost effective ways to enhance the robustness of the loopback test scheme

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